Abstract

IDEC Chip Design Contest

Pseudo-Static n-type Gain Cell of Embedded DRAM for Processing-in-Memory Application

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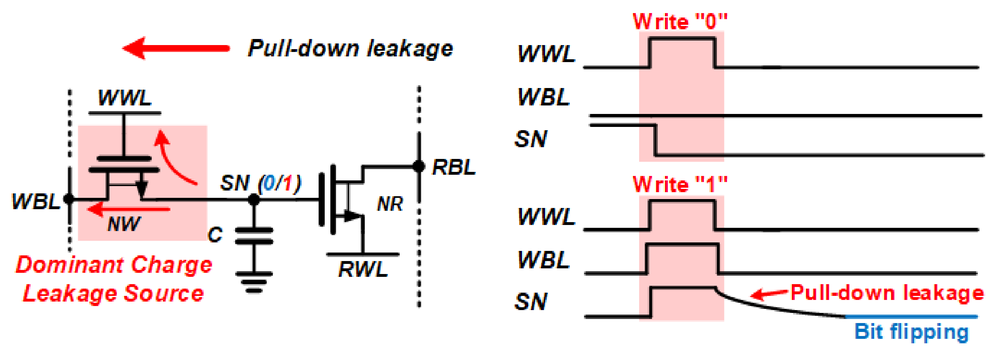
Abstract

This article proposes a pseudo-static n-type gain cell (PS-nGC) that can achieve an extended data retention time without requiring refresh operations. The proposed PS-nGC for embedded dynamic random-access memory (eDRAM) macro can be utilized in analog processing-in-memory (PIM) applications by storing data without charge loss through leakage compensation.

Data Retention Time Issue

• **In a conventional 2T1C cell,** there are two transistors and one capacitor, and the retention time of data stored in the storage node (SN) is mainly dependent on the capacitor and the leakage current through M1 and M2. To enhance the usage of gain-cell in PIM applications, the retention time for storing data "1" needs to be extended by compensating for the leakage current of M1.

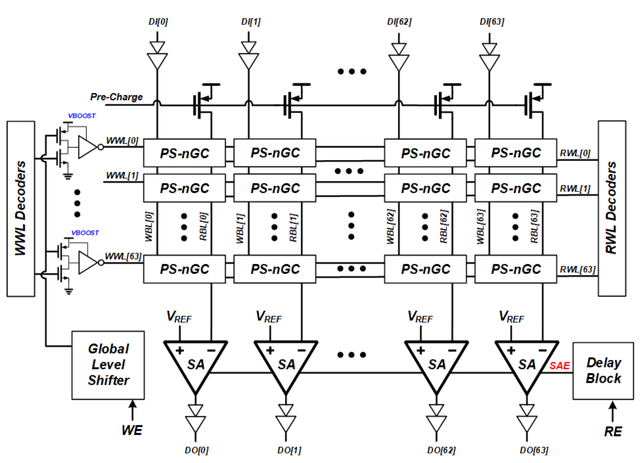


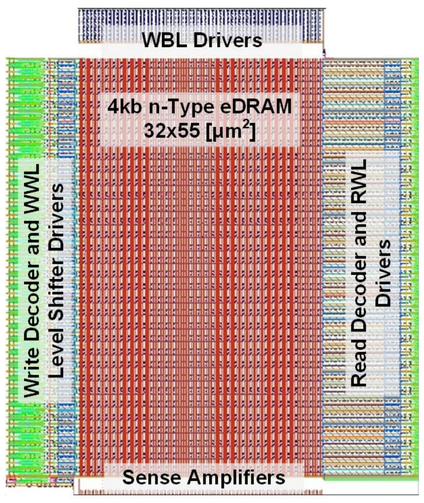
Proposed Design

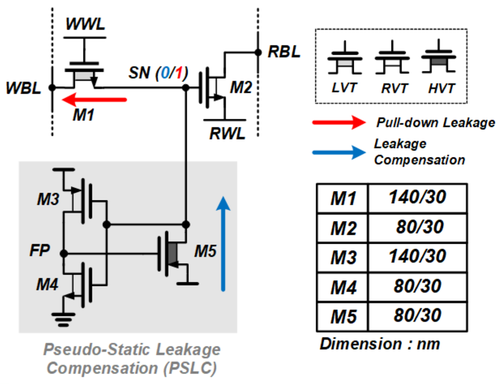
• **The proposed PS-nGC eDRAM macro** consists of 64 x 64 cells, 64 x differential sense amplifier and peripheral circuits.

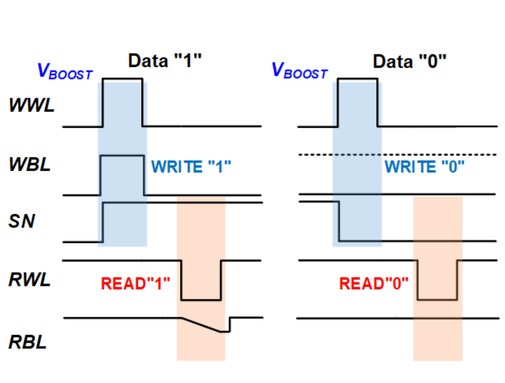
• **The PS-nGC** consists of a conventional 2T gain cell and PSLC. PSLC can actively compensate for the charge loss that affects SN, enabling data preservation.

• **The PSLC** is activated when SN stores data “1”. By pulling up the leakage current through the PSLC, SN can hold data “1” without increasing the voltage.





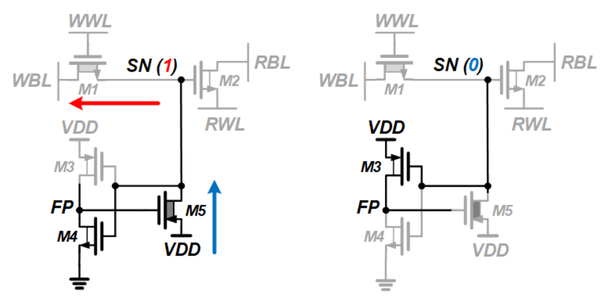




Detailed Operation

• **The Data hold mode**

- *If SN stores data “1”*, M3 turn off and M4 turns on, thereby making M5 compensate the leakage current. Then, M5 forces the SN to be VDD by pulling up the residual charge injected through M1 and M2.
- *If SN stores data “0”*, only M3 turns on, and the feedback path (FP) node is forced to be VDD. Therefore, M5 turns off, and SN can maintain its voltage without significant charge loss.

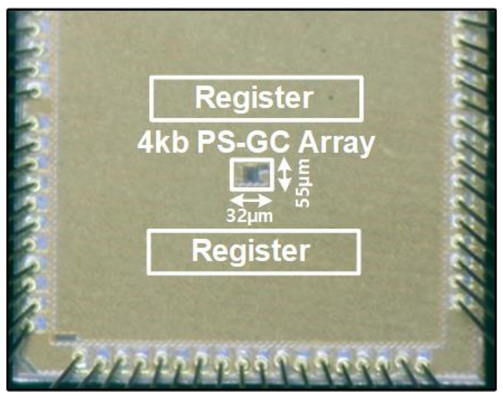


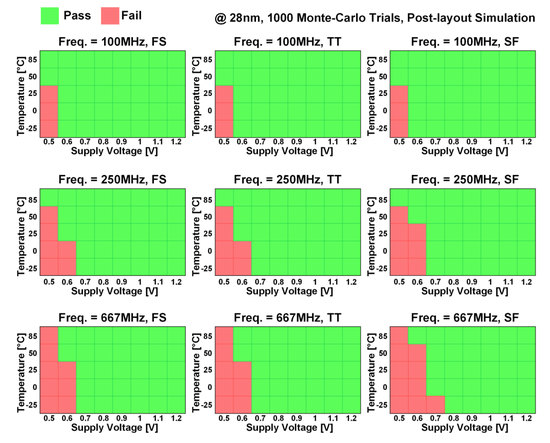
Simulations

• After writing data, the PSLC successfully enabled the gain cell to maintain the stored voltage.

• The area of the eDRAM macro based on the PS-nGC implemented in 28nm CMOS process is 0.43 μm × 0.66 μm (0.284 μm²).

• At the operating frequency of 667 MHz, the eDRAM macro achieved an operating voltage range from 0.8V to 1.2V and operating temperature range from −25 to 85 ◦C regardless of the process variation.





Conclusions

In this article, the PS-nGC is proposed to overcome the data retention time issue of eDRAM. The PS-nGC extends data retention time without capacitors. As a result, the PSLC actively compensates for charge loss even in the 28nm process, which has a severe sub-threshold leakage. Therefore, the proposed PS-nGC based eDRAM macro is expected to be applied to analog PIM.

Reference

Subin Kim and Jun-Eun Park, "Pseudo-Static Gain Cell of Embedded DRAM for Processing-in-Memory in Intelligent IoT Sensor Nodes," *Sensors*, vol. 22, no. 11, pp. 4284, Jun. 2022.

Acknowledgement

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